Integrating III-V on Silicon for Future Nanoelectronics

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Since the early 2000's, silicon manufacturers have been exploring many new electronic materials and incorporating them into silicon CMOS transistors to boost their device performance and enhance their energy efficiency. For instance, the use of Hf-based gate dielectric and dual work-function metal gate electrodes to replace SiO_2/polySi as the gate stacks in the current 45nm technology node, which started volume production in 2007, has been considered as the biggest change to the silicon transistor in 40 years [1, 2]. Going forward it is expected that the trend of incorporating more new materials into CMOS transistors will continue, and that more non-silicon materials, possibly including III-V materials, will be integrated onto the silicon substrate in future technology nodes [3].

Recently there has been much interest generated and good progress made in the research of low band-gap III-V compound semiconductors to replace silicon as the future transistor channel material to enhance device performance and reduce power consumption. For instance, both InSb and InGaAs quantum-well field effect transistors [4, 5] have shown significantly improved transistor energy-delay product, which represents the energy efficiency of the transistor, over standard silicon n-channel MOSFETs, as shown in Figure 1 [3]. However, for III-V compound semiconductors to become applicable to the silicon industry, they will need to be integrated onto large silicon wafers. A seamless, robust heterogeneous integration scheme of III-V on silicon will allow high-speed, low-voltage III-V based transistors to couple with the mainstream Si CMOS platform, while avoiding the need for developing large diameter (≥ 300mm) III-V substrates. Besides transistor applications, successful integration of III-V on silicon can open up opportunities for integrating new functionalities and features on silicon, such as integrating logic, optoelectronic and communication platforms on the same Si wafer.

While III-V transistors have shown some very attractive and tangible merits, many technical challenges need to be overcome before they will become practical for future high-speed and low-power digital applications [6]. So far good progress has been made by various research groups in industry and academia in tackling these difficult challenges. For instance, the recent demonstration of high performance and low power enhancement-mode $In_{0.7}Ga_{0.3}As$ quantum-well transistor on silicon substrate via a thin composite metamorphic buffer layer, as shown in Figure 2 [7], has generated much excitement in both the silicon and III-V research communities. This presentation will describe our vision on III-V integration on silicon and summarize the recent progress on the research efforts to combine the merits of III-V and silicon, on the same silicon wafer, for future high-speed and low-power nanoelectronics. In addition, it will address the challenges that need to be overcome.

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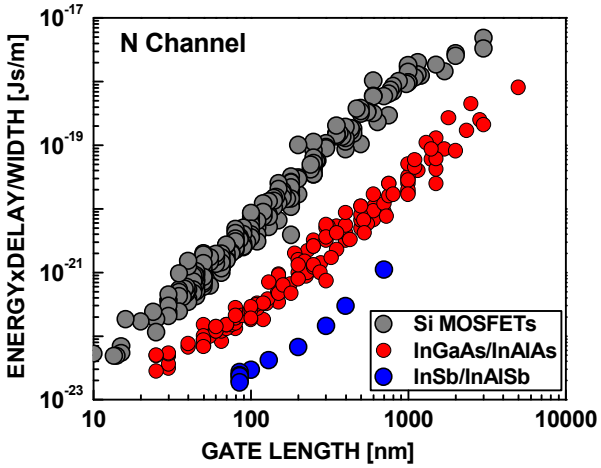

Figure 1: Normalized energy-delay product of n-channel InSb and InGaAs quantum-well transistors compared with that of standard silicon MOSFETs [ref. 3].

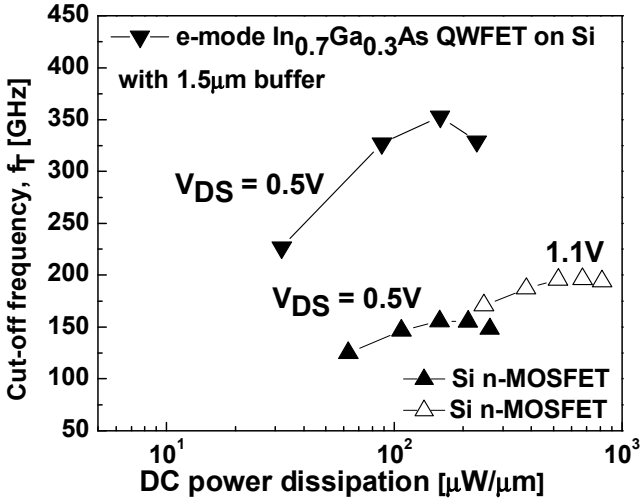

Figure 2: Cut-off frequency as a function of DC power dissipation for the enhancement-mode L_G=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.5μm composite buffer at V_{DS}=0.5V, versus standard Si n-MOSFET transistor with L_G = 60nm at V_{DS}=0.5V and 1.1V [ref. 7].